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THE PROGRESS OF RESEARCH AND DEVELOPMENT OF INTEGRATED FERROELECTRICS

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Abstract

The progress in terms of processing technology and electrodes for the PZT and SBT ferroelectric capacitors in FERAMs is reported. The key issues addressed for BST films in DRAMs are presented. The ferroelectric materials used in microwave devices are illustrated. Antiferroelectric materials used in microelectro-mechanical systems are briefly discussed. The work in modeling Metal-Ferroelectric-Semiconductor Field Effect Transistor is summarized. It is recommended that the research and development of MFSFETs and their application in nonvolatile memories should be further pursued.

Introduction

PZT and SBT ferroelectric thin films are the major materials used in FeRAM. The major difficulties to integrate the ferroelectric material to silicon VLSI fabrication processes came from the degradation of the ferroelectricity in such materials during the fabrication. The progress has been made in terms of processing technology and electrodes for the ferroelectric capacitors.

As of 1996 there were three main problems for integration of SBT film. They were: (1) it had high processing temperatures, (2) it needed barrier materials for bottom electrodes which stopped the diffusion of Bi, and (3) the limitation of lateral cell sizes. According to a paper the first two problems were solved; the third problem is still not solved [1].

Based on the Proceedings of the Tenth International Symposium on Integrated Ferroelectrics, the efforts of the integration of SBT films were focused on processing technology and electrodes for the SBT thin film capacitor.

Several deposition techniques for SBT thin films have been reported, such as PEMOCVD [2], RF magnetron sputtering [3], MOCVD [4], low temperature preparation of the SBT film by

a modified RF magnetron sputtering technique [5], chemical solution deposition [6], photosensitive MOD solution [7]. The other processing innovations included recovery anneal after deposition of the PT top electrode [8], annealing in sol-gel derived SBT films [9], Rapid Thermal Annealing (RTA) on SBT film [10]. The other topics under study for SBT films include: imprint in SBT capacitors [11]; the memory effects of SBT films deposited on Si substrate with an ultra-thin silicon nitrate buffer layer [12]; the relation between the electrical properties and the microstructure of SBT film [13]; Schottky-limited and space-charge-limited current in SBT-PT contacts [14]; and the role of abnormal grain growth on the SBT films [15].

For PZT a lot of efforts have been made to overcome its shortcomings such as fatigue. A variety of electrode materials have been used for PZT [16] for this purpose. The La and Nb modification of PZT was the other method to solve the switching fatigue problem for PZT [17]. The PZT ferroelectric properties also heavily depend on the electrode processing condition [18]. The use of noble metal electrodes such as Pt caused polarization fatigue in PZT capacitors. The conductive oxide materials have been used as electrodes for the PZT capacitors in nonvolatile random access memories such as IrO_2 [19,20,21], $La_{0.5}Sr_{0.5}C_0O_3$ [21,22,23], $YBa_2Cu_3O_7$ (YBCO) [21,22], RuO_2 [21,23] and $SrRuO_3$ [18,21]. On the other hand Pt/PZT/Pt capacitors have been continuously studied by using various annealing techniques to investigate its degradation mechanism [24]. The degradation of ferroelectric properties caused by annealing in a reductive ambience was studied for using different materials than Pt, such as IrO_2 which was used as a top electrode for the capacitor [20]. The role of the top electrode to the depreciation of ferroelectricity of PZT capacitors has been investigated. The effect of N_2-H_2 annealing on Pt/PZT/Pt capacitors has been studied [24].

BST is the material widely used for the giga-bit scale dynamic random-access memories (DRAMs), and on-chip capacitors for RF devices. The advantages of using BST are (1) it has high dielectric constant even at high frequency range (GHz), (2) it has good thermal stability, (3) it has very good insulating property, and (4) it has low leakage current and low dielectric loss [25,26,27]. The first key issue for process integration of BST capacitors is concerned with the selection of bottom electrodes. The second issue deals with the BST film deposition process which depends on the bottom electrode material and the capacitor structure. The third key issue is about the diffusion barrier under the bottom electrodes, which is needed to prevent the electrodes from degradation through reaction with poly-Si plug in the process of BST deposition and post annealing [28,29,30,31,32,33].

BST can be used in microwave devices too [34,35,36,37]. Based on the electric field dependence of the dielectric constant, ferroelectric thin films were used in tunable microwaves devices and circuits [34,37]. $Ba_{0.5}Sr_{0.5}TiO_3$ and $Ba_{0.6}Sr_{0.4}TiO_3$ had demonstrated to be promising in this area. In the last few years, a very good progress has been made for deposition of BST thin films with high dielectric tunability and low microwave losses. One of the issues in the development of microwave devices by using ferroelectric materials is the dielectric losses (the loss tangent tanδ) [34,35]. The processes of deposition, annealing, and doping had been optimized to reduce the losses in the microwave region. The other issue is the variations of dielectric constant and dielectric losses due to the elevated microwave power levels. [36].

In the last several years the ferroelectric thin films have also been applied in microelectro-mechanical systems (MEMS). PZT films, which have strong piezoelectric effect after poling, have been playing an important role in this area. The disadvantages of using PZT in MEMS include the significant hysteresis of electric field-induced displacement, aging and

fatigue. Ferroelectric relaxor materials such as a composition of lead magnesium niobate titanate, 0.9 Pb $(Mg_{1/3}Nb_{2/3})O_3$ – 0.1 $PbTiO_3$ (PMN-PT), are good replacements of PZT films. They have a high dielectric constant and piezoelectric coefficient, which are tunable by a dc bias voltage. They also have a high elastrostrictive strain. They do not show hysteric property. The frequency dispersion of PMN-PT film is small, which makes the materials useful in high frequency microelectro-mechanical devices [38].

Antiferroelectric materials in the lead zirconate titantate stannate family, such as $Pb_{0.99}Nb_{0.02}$ $(Zr_{0.85}Sn_{0.13}Ti_{0.02})_{0.98}O_3$ (abbreviated as PNZST) and $Pb_{0.97}La_{0.02}$ $(Zr_{0.65}Sn_{0.31}$ $Ti_{0.04})O_3$ (abbreviated as PLZST) were used for high-strain microactuators. All the films can have either square hysteresis loop or slanted hysteresis loop. For the former the antiferroelectric-to-ferroelectric phase transition occurs as a step function of electric field, and allows for digital applications. For the latter, the phase transition occurs gradually with electric field and allows analog applications. These antiferroelectric thin and thick films are useful for microactuation applications in microelectro-mechanical systems [39].

The Improvement of PZT Capacitors in FeRAMs

PZT is still a very important ferreoelectric thin film used for FeRAM. The major difficulties of integrating ferroelectric capacitors on a scale larger than 1Mb by using conventional CMOS process come from the degradation of ferroelectricity of the material. The PZT capacitors were degraded in a hydrogen-containing atmosphere [40].

The mechanism for the degradation of a PZT capacitor was investigated on the Pt/PZT/Pt capacitor. The relationship of the degradation to hydrogen annealing condition with various hydrogen pressures and temperature was studied. It was found that nonvolatile polarization (Pnv) was reduced with higher hydrogen partial pressure and temperature. Hydrogen atoms in

PZT increased while the number of oxygen atoms decreased in the upper Pt electrode after N_2-H_2 annealing. The increase of hydrogen content in PZT caused the decrease of the nonvolatile polarization. The voltage shift of hysteresis was induced by the N_2-H_2 annealing. It was understood that the defect content (such as oxygen vacancies) of PZT was related to the hydrogen content, which was the cause of a voltage shift. However, there was no clear correlation between the nonvolatile polarization and the oxygen content. The adhesion of Pt/PZT was affected by the amount of oxygen in Pt. The reduced amount of oxygen in Pt made the adhesion of Pt/PZT worse. In short, in the process of annealing in a hydrogen-containing atmosphere the degradation of a PZT capacitor was due to the absorption of H_2 molecules to the catalyzer surface of the Pt electrode and were decomposed into atomic hydrogens which deoxidized the PZT. This was the reason why a Pt/PZT/Pt capacitor deteriorated in its ferroelectricity by H_2 annealing even at the annealing temperature as low as 300°C, or less.

The mechanisms of the adhesion of Pt/PZT and the hydrogen trapping formed in PZT need further investigation. In the future the electrode used should not generate radical hydrogen and the ferroelectric material should not be reduced with forming gas annealing [39].

The H_2 degradation could be eliminated by using IrO_2 top electrode. IrO_2/PZT/Pt capacitors were fabricated [41]. These capacitors were resistant against the H_2 annealing up to 400°C. An oxygen annealing of IrO_2/PZT/Pt ferroelectric capacitors at temperatures from 400° to 600°C was performed to increase the degree of oxidation of IrO_2 and to make the capacitors more resistant against the H_2 annealing. It was proved that IrO_2/PZT/Pt capacitors were effective to avoid H_2 damage in the LSI processes [41].

The PZT capacitor characteristics were affected by deposition process of the top electrode. The deposited film structure of Ir or IrO_2 was related to the sputtering conditions,

such as the DC power and the O_2 pressure in the plasma gas. High oxygen pressure and lower substrate temperature, such as 200°C, for IrO_2 sputtering resulted in higher values of Pr (Pr represents remanent polarization). PZT capacitors with a target of Zr/Ti = 0.35/0.65 were fabricated at low temperature (200°C) and high oxygen pressure. These capacitors had a wide operational margin ΔV_B($\Delta V_B = V_{BS} - V_{BN}$, where V_{BS} represents the "switching" bit-line voltage while V_{BN} represents the "non-switching" bit-line voltage) [42].

Although the Ir based top electrode was used to improve the fatigue and imprint characteristics for PZT films. This kind of top electrode alone was not enough to stop the degradation of the device, which was resulted from stress in the high temperature and high humidity. The adequate passivation for the ambience was needed to prevent this degradation from happening. SiN based passivation over the Al wired layer was introduced, which has better effect than using the SiO_2 based passivation [20].

Besides using oxide materials such as IrO_2 and RuO_2 as electrodes to combat against fatigue in PZT, the dopings of La, Nb and Sb in PZT films were employed. The grain sizes of the undoped PZT were smaller than those doped with Sb. The latter shows the improvement of the fatigue properties of the PZT films. The shape of the hysteresis loop and the remanent polarization increased from 11 $\mu c/cm^2$ of undoped PZT to 32 $\mu c/cm^2$ of the 0.7% doped PZT. In addition, the shapes of the hysteresis loop before and after fatigue tests (10^{10} cycles) changed less for the doped PZT films, which demonstrated improved fatigue properties [43].

Besides using the Ir based top electrodes electrical properties of PZT thin films grown on Ir/IrO_2 bottom electrodes by MOCVD, such as $Ir/IrO_2/PZT/Ir/IrO_2$ and $IrO_2/Ir/PZT/Ir/IrO_2$ were studied. Because of plasma damage during top electrode sputtering $Ir/IrO_2/Ir/PZT/Ir/IrO_2$ capacitors did not have good electrical properties. But there was no fatigue up to 10^9 cycles for

IrO_2/Ir/PZT/Ir/IrO_2 which was annealed after top electrode deposition. The electrical properties of IrO_2/Ir/PZT/Ir/IrO_2 capacitors were affected by Ir/IrO_2 bottom electrode which acted as a good barrier layer of interdiffusion [44].

The fabrication of nonvolatile ferroelectric random access memory (NVFRAM) using PZT films with silicon substrates required good integration of these two materials. Progress was made in low temperature growth and orientation control in MOCVD PZT/RuO_2 thin films heterostructures on SiO_2/Si substrates. The orientation of the PZT film strongly depended on the orientation of RuO_2 bottom electrode layers. The orientation of RuO_2 electrode could be controlled by adjusting the growth rate and substrate temperature. It was shown that PZT films could be grown on RuO_2/SiO_2/Si substrates by MOCVD at about 525°C and had very good ferroelectric properties [44].

PZT capacitors used $SrRuO_3$ (SRO) and La-Sr-Co-O (LSCO) exhibited less fatigue compared to Pt electrodes. The PZT ferroelectric behaviors were substantially affected by the SRO bottom electrode processing conditions. The SRO/Pt bottom electrodes were deposited at 600°C and at lower temperature, followed by annealing at 600°C.. The advantages of using SRO electrodes are that it could make the coercive fields smaller and could enhance perovskite nucleation [45].

The Progress of SBT Films for Non-Volatile Ferroelectric Memory Applications

There is no significant fatigue for strontiium-bismuth-tantalate ($SrBi_2Ta_2O_9$) thin films after 10^{12} switching cycles. It is known that PZT grown on Pt/Ti electrode has fatigue problems which made the ferroelectric memories able to stand only limited number of switching cycles. The SBT-based capacitors, even integrated with Pt electrodes, showed negligible fatigue and imprint.

As of 1996 there were three main problems for integration of SBT film. The first was that it had high processing temperature, the second was that it needed barrier materials for bottom electrodes which stopped Bi diffusion, and the third problem is the limitation of lateral of cell sizes. The first two problems were solved by mid-1997. Cell sizes are still the problem of developing high-density storage memories. As of 1998 the smallest functional SBT cells are those of $0.7\times0.7\ \mu m^2$ from NEC, the $0.1\times0.1\ \mu m^2$ Bi and Bi_2O_3 self-patterning electrodes may be able to solve the last of these problems [1].

SBT films were successfully prepared on $Pt/SiO_2/Si$ and $Pt/Ti/SiO_2$ substrates at 550°C by plasma-enhanced metalorganic chemical vapor deposition (PEMOCVD). A $Bi_2Ti_4O_{11}$ (BTO) phase was formed at the interface between SBT films and $Pt/Ti./SiO_2/Si$. The leakage current density of the SBT films decreased due to the formation of the BTO phase. The leakage current can be calculated using the following equation:

$$\ell n[\Delta(J/T^2) = \frac{q\Phi_B}{k} \cdot \left[\Delta\left(\frac{1}{T}\right)\right]$$

where Φ_B is the Schottky barrier height, J is the leakage current density, T is temperature, q is the electronic charge and k is the Boltzmann constant. The Schottky barrier of SBT films deposited on $Pt/Ti/SiO_2/Si$ was 1.2 eV while the barrier height of the thin films on $Pt/SiO_2/Si$ was 0.8 eV [2].

Second, the SBT films were deposited on 6-inch $Pt/Ti/SiO_2/Si$ substrates by RF magnetron sputtering, which was easier to operate and compatible with current silicon LSI processes. The Bi content in the SBT films can be varied by changing the deposition parameters such as RF power and Ar gas pressure during SBT sputtering. It has been observed that the temperature needed to have a good hysteresis loop is lowered by increasing the Bi content [15].

A low temperature MOCVD process for SBT using Bi $(thd)_3$ as Bi source was introduced. It fabricated the SBT films with high remanent polarization (25 $\mu c/cm^3$), the low coercive voltage (0.55 V). This made the SBT films useful for high density and low power FeRAMS (16 M and above). This process allowed deposition temperatures down to 300°C [4]. Along this line a process using chemical solution deposition of the SBT films at low temperature was reported [6].

The structural and electrical degradation was shown in SBT films after a forming gas (5% H_2, 95% N_2) annealing. This made an additional oxygen annealing necessary to reduce the degradation of ferroelectricity in the SBT films. The SBT films were made by a sol-gel technique using complex methoxyethoxides [55]. The mechanism for the degradation was proposed. It stated that during the initial oxygen anneal at high temperatures, the bismuth diffused out of the SBT film and alloyed with the underlying platinum electrode. The hydrogen reduced bismuth to its elemental state as the sample was annealed in the forming gas. Since platinum could act as a catalyst for breaking down hydrogen molecules to hydrogen atoms, bismuth was further reduced. Furthermore, liquid bismuth was formed in the annealing step, which diffused to the platinum layer and caused the growth of the tall bismuth-platinum towers. The conclusion of this study was that platinum is too reactive with bismuth at the high processing temperature (up to 700°-800°C). Therefore, platinum was not an effective electrode for SBT films in integrated ferroelectric structure. It was recommended that other materials, such as ruthenium, iridium, and their oxides are used as the electrodes for SBT films [54].

The ferroelectric properties of SBT films were optimized by using Rapid Thermal Annealing (RTA). There were two steps for the Rapid Thermal Annealing. In the first step the SBT films were annealed at 700°C for 30 seconds at ramp rates between 75 to 125°C/sec. In the

second step the SBT films were annealed in a diffusion furnace at 800°C for 30 to 60 minutes [48,55].

The other effective way to prepare the SBT film is to use chemical solution deposition (CSD). The strategies used to optimize the properties of the films include the variation of the composition of the SBT films, the change of the annealing temperature for the substrates, the choices of different metallization materials such as Pt, Ir, and IrO_2 metallizations, and the optimization of the thermal processing cycle. A 1700 Å SBT film was prepared by this method, which has a switchable polarization greater than 10 $\mu c/cm^2$ and an operating voltage less than 2.0 V [53].

The relation between the ferroelectric properties and the crystal structure of the SBT films were studied. The nonstoichiometric SBT thin films with molar ratio (Sr:Bi:Ta) of 1:2:2, 0.7:2.2:2, 1.87:2.2:1.93, 1:2.2:2 and 0.7:2:2 were prepared by MOD spin coating. Remanent polarization of the thin films depended on the cyrstallinity and grain size. The 0.7:2.2:2 thin films showed the best ferroelectric properties. Nonstoichiometric SBT thin films showed better ferroelectric properties than stoichiometric SBT thin films did [49].

Stoichiometric $SiBi_2Ta_2O_9$ (SB)-Pt contact was expected to be a Schottky contact with a barrier height of 0.9 eV. But the diffusion of excess-Bi in the SBT films into the Pt electrodes can change the SBT-Pt contact to ohmic contacts at low voltage. In this case space-charge-limited current dominated by the electronic conduction mechanism in Bi-rich capacitors, instead of the Schottky emission current. It can be calculated by

$$J(E) = AV / d + B(V - V_0)^2$$

where V_0 is the trapping potential for the principal impurities in the ferroelectric film. A is related to bulk property. B is the function of the trap densities of electrode-ferroelectric

interface, and it also depended on the other conditions of the interface. For the current-temperature relationship Rose's theory gives a good explanation [50].

Pt top electrodes were used for SBT capacitors, but there were no hysteresis loop after patterning of the Pt/SBT stack. In order to have hysteresis loops for the SBT films, recovery annealing with temperature higher than 600°C was necessary. The recovery annealing was studied as a function of temperature and time. It was found that annealing temperature higher than 700°C made low leakage current possible. For example, a leakage current of less than 10^{-7} A/cm^2 was obtained at 800°C [7].

The Progress of BST for Memory Applications

To fabricate giga-bit scale DRAMs the capacitors used high dielectric constant materials. $Ba_{1-x}Sr_xTiO_3$ (BST) has high permittivity, stability, and high temperature resistance. Extensive research has been focused on the integration of BST with silicon. The important issues for process integration are electrode materials, barrier layers, and the improvement for BST films themselves [56].

The first issue is concerned with the selection of bottom electrodes. The materials used for bottom electrodes include Pt, Ir, IrO_2/Ir, Ru, and RuO_2/Ru. Pt, Ir and IrO_2/Ir had difficulties for controlling the profiles and feature sizes in dry etching,. However, these difficulties did not exist for the etching of Ru and RuO_2. When Ir was used as electrode material it has very good adhesion to SiO_2, and served as a good barrier to oxygen diffusion. BST capacitors with Ir electrodes demonstrated larger values of capacitance and smaller values of leakage current densities [57]. However, the materials such as platinum, ruthenium, ruthenium oxide, and iridium oxide have the disadvantages of high costs, difficulties in dry etching processing and generation of highly toxic gases formed during the reactive ion etching (RIE) processing of these

materials. The new bottom electrodes used a metallic buffer in a capacitor stack which was built on TiN/Si (100) substrates. This new capacitor stack built on Au/BST/M/TiN/Si was integrated to silicon for DRAMs [56]. The dielectric constant and the leakage current density of BST films with different bottom electrode materials were studied before and after annealing in O_2 ambient. The post annealing process after deposition affected the crystallinity and electrical properties of BST films deposited on Pt, Ir, IrO_2/Ir, Ru, and RuO_2/Ru bottom electrodes. The dielectric constant, the loss tangent and the leakage current of the BST film were affected by annealing in O_2 [58].

The second issue deals with the BST film deposition process. This process depends on the bottom electrode material and the capacitor structure.

The third issue is related to the diffusion barrier under bottom electrodes, which is needed to prevent the electrodes from degradation through reaction with poly-Si plug in the process of BST deposition and post annealing.

To deal with the oxidation of barrier layers a two-step post-annealing was used. It included the annealing which was carried out at 650°C under vacuum atmosphere, and subsequently at 400°C under the oxygen atmosphere. This process was designed to prevent the barrier oxidation. In addition a concave-type capacitor structure with buried barrier using Pt electrodes was proposed. The barrier material CVD-TiN was buried to prevent the direct contact of BST and the barrier layer [59].

Patterning of Pt as a bottom electrode has its difficulties which were overcome by etching thin Pt in the sidewall. An effective thick Pt bottom electrode was subsequently made. The yield of breakdown voltage of the BST capacitor was thus improved due to the optimization of the profile of the bottom electrode. Besides, doping the Pt electrode with oxygen resulted in a

substantial reduction of the leakage current of the BST capacitor and made the capacitor immune to the attack of the reducing plasma [60].

Some theoretical studies were also carried out for the high-dielectric constant capacitors such as the BST capacitor. The maximum interface capacitance between BST and the electrodes could be estimated by using a theoretical model. Based on the theoretical estimation the maximum achievable capacitance per unit area for a Pt/BST/Pt capacitor is only 250 $fF/\mu m^2$, which was not enough for a 1 G-bit DRAM device. Based on this theoretical study it was concluded that the choice of electrode materials may become as important as the choice of insulators [61]. Time dependent dielectric breakdown and stress-induced leakage current for BST thin films were also investigated [62].

Barium Strontium Titanate (BST) is a ferroelectric material with low Curie temperature. For the ferroelectric materials used for non-volatile memories, such as lead zirconate titanate (PZT) and strontium bismuth tantalate (SBT), the Curie temperatures are above 200°C, but the Curie temperature of BST is below 130°C. However, the Curie temperature can be changed by applying mechanical stress. For example, the application of two-dimensional compression results in the crystal deforms in the perpendicular direction and the space for ionic displacement of titanium. The Curie temperatures for the materials subsequently became higher. In this paper the Curie temperature due to two-dimensional stress was calculated by a polynomial function of polarization P:

$$G = \frac{1}{2}xP^2 + \frac{1}{4}\varepsilon_{11}P^4 + \frac{1}{6}\varepsilon_{111}P^6 - 2Q_{12}HP^2$$

where H represents bi-axial stress and Q_{12} is an electrostriction coefficient.

Lattice misfit between the BST film and the substrate results in two-dimensional stress. The BST films and $SrRuO_3$ films were prepared by rf-magnetron sputtering. $SrRuO_3$ films were

also epitaxially grown on $SrTiO_3$. The lattice misfit was controlled by Ba/Sr ratio in the BST films. When the barium content was increased the remanent polarization was also increased. The remanent polarization reaches the maximum value with 70% barium content. It was concluded that Curie temperature of heteroepitaxial BST films can be raised to higher than 200°C. It was also possible to grow heteroepitaxial BST films on silicon substrate. Heteroepitaxial BST films can be applied to non-volatile memories. The advantages of using theses BST films are:

1. They are chemically stable because they do not contain Pb or B.
2. BST films are compatible with silicon process because they are resistant to reducing atmosphere such as H_2 or N_2.
3. The thickness of BST films can be scaled to 20 nm.

Therefore, the heteroepitaxial BST film is a good candidate which can be applied to high-density integration for non-volatile FRAMs [63].

The Application of Thin Film Ferroelectrics to High Frequency Devices

The ferroelectric material could be used in microwave devices. Strontium titanate ($SrTiO_2$, STO), barium titanate ($BaTiO_3$, BTO) and solid solution of STO and BTO (BSTO) were used in electrically controllable microwave devices. The high microwave loss of these materials were one of the problems. $YBa_2Cu_3O_{7-x}$ (YBCO), a high temperature superconductor, has structural compatibility with STO. Single crystal STO or $KTaO_3$ (KTO) and thin epitaxial films of STO and BSTO were integrated with high temperature superconductors. The bulk ferroelectric devices were applied in wireless communication systems which operated at cryogenic temperatures in the frequency range 0.2-2.0 GHz. Ferroelectric thin film devices were used in these systems at room or cryogenic temperature in the frequency range 1-40 GHz and

higher. In order to use the ferroelectric material for the microwave devices, there is a need to address the problems such as the relation between the interface of ferroelectrics and conducting/superconducting electrodes and the microwave loss, the interdiffusion of Ba in the system of STO/YBCO, the mechanical stress and the nature of the electrode/ferroelectric contact [64].

STO/YBCO structures found their applications in coplanar waveguide devices (CPWs). The STO was used as a nonlinear dielectric medium. A bias voltage was applied to $SrTiO_3$ nonlinear dielectric. As a result an electric field was created in the dielectric material to tune its nonlinearity. The effect of noise on the mixed microwave output was also studied in the same STO/YBCO coplanar waveguide devices. It was demonstrated that the STO thin film showed strong nonlinearities which were useful for microwave solitons and stochastic resonance [65]. Microwave solitons are formed when a specific dispersion is used to counteract the nonlinearity effects of certain waveforms. Stochastic resonance is a phenomenon in which random noise is used to enhance a nonlinear response of the system to a weak periodic signals.

The microwave components using gold, YBCO/STO/LAO (conductor/ferroelectric/ dielectric) thin film multiple-layer structures could be applied to Ku and K-band satellite communications [66]. Even at the current level of development the nonlinear dielectric STO layers with superconducting YBCO electrodes could be used advantageously in satellite and wireless communication systems for Ku- and K-band operation. $SrTiO_3$ (STO) and $BaTiO_3$ (BTO) could be optimized to make low cost frequency agile technology at room temperature possible.

$YBa_2Cu_3O_{7-x}/SrTiO_3/LaAlO_3$ (YBCO/STO/LAO) and $Au/SrTiO_3/LaAlO_3$ (Au/STO/ LAO) were used as microwave phase shifters. The advantages of using these ferroelectric thin

films were light weight, compact, very low power, and voltage tunable. However, the microwave losses of these ferroelectric materials were still too large. The phase shifters of these microstrip-based Conductor/Ferroelectric Thin Films were optimized to make microwave losses smaller and to make relative insertion phase shift larger [67].

BST was used in tunable microwave devices such as voltage tunable phase shifters, oscillators, filters, and parametric amplifiers. One of the problems of using BST for microwave devices was a high loss tangent. BST with various dopants were investigated. The dielectric properties between laser-ablated Mn-doped BST and undoped BST were compared at microwave frequencies. It was found that BST films doped with one atomic percent of Mn had a dielectric constant as high as 1820, a tunability of 56% at 40 kV/cm DC electric field and a loss tangent of 0.006 at zero bias at the frequency of 10 GHz at room temperature [68].

Modeling of Metal-Ferroelectric-Semiconductor Field Effect Transistors

This section is concerned with the contribution of Todd C. MacLeod and the author of this report, Fat Duen Ho, in Modeling Ferroelectric-Semiconductor-Field Effect Transistors. The characteristics of a MFSFET (metal-ferroelectric-semiconductor field effect transistor) is very different than a conventional MOSFET and must be modeled differently. The drain current has a hysteresis shape with respect to the gate voltage. The position along the hysteresis curve is dependent on the last positive or negative polling of the ferroelectric material. The drain current also has a logarithmic decay after the last polling. A model has been developed to describe the MFSFET drain current for both gate voltage on and gate voltage off conditions. This model takes into account the hysteresis nature of the MFSFET and the time dependent decay. The model is based on the shape of the Fermi-Dirac function which has been modified to describe the

MFSFET's drain current. This is different from the model proposed by Chen et al. And that by Wu [69].

The ferroelectric channel in a Metal-Ferroelectric-Semiconductor Field Effect Transistor (MFSFET) can partially change its polarization when the gate voltage nears the polarization threshold voltage as shown by Aizawa. This causes the MFSFET drain current to change with repeated pulses of the same gate voltage near the polarization threshold voltage. A previously developed model. Based on the Fermi-Direct function, assumed that for a given gate voltage and channel polarization, a single drain current value would be generated. The earlier model accurately predicts the drain current given a series of increasing and decreasing pulses, but does not predict the current well for a series of random pulses. A study has been done to characterize the effects of partial polarization on the drain current of a MFSFET. These effects have been described mathematically and these equations have been incorporated into a more comprehensive mathematical model of the MFSFET. The model takes into account the hysteresis nature of the MFSFET and the time dependent decay as well as the effects of partial polarization. It can accurately calculate the drain current given any random series of gate pulses in both time and voltage. This model defines the drain current based on calculating the degree of polarization from previous gate pulses, the present gate voltage, and the amount of time since the last gate voltage pulse [70].

The details of the modeling of Metal-Ferroelectric-Semiconductor Field Effect Transistors are in Appendix I and Appendix II.

Summary and Conclusion

A lot of efforts have been made with success to overcome the degradation of the ferroelectricity in PZT and SBT to integrate these ferroelectric films to silicon VLSI fabrication

processes. PZT capacitors used $SrRuO_3$ (SRO) and La-Sr-Co-O (LSCO) exhibited less fatigue compared to Pt electrodes. The H_2 degradation for PZT films could be eliminated by using IrO_2 top electrode. IrO_2/PZT/Pt capacitors were resistant against the H_2 annealing up to 400°C. The Ir based top electrode was used to improve the fatigue and imprint characteristics for PZT films. In addition, SiN based passivation was needed to prevent the degradation of ferroelectricity.

The disposition temperature for SBT films got lower. SBT films were successfully prepared on Pt/SiO_2/Si substrate at 550°C by PEMOCVD. A MOCVD process was used to deposit SBT films at 300°C. Along this line a process using chemical solution deposition of the SBT films at low temperature was reported. It was found that platinum was not an effective electrode for SBT films. Other materials, such as ruthenium, iridium, and their oxides were used as the electrodes for SBT films. The strategies used to optimize the properties of the films inlcude the variation of the composition of the SBT films, the change of the annealing temperature for the substrates, the choices of different metallization materials such as Pt, Ir, and IrO_2, and the optimization of the thermal processing cycle. It was found that the ferroelectric properties of the SBT films depended on the molar ratio (Sr:Bi:Ta). The annealing also played an important role to improve the ferroeoelctric properties of SBT films.

The important issues for the integration of BST films are electrode materials, barrier layers, and the improvement for BST films themselves. The materials used for bottom electrodes include Pt, Ir, IrO_2/Ir, Ru, and RuO_2/Ru. Based on the theoretical estimation the maximum achievable capacitance per unit area for a Pt/BST/Pt capacitor is only 250 $fF/\mu m^2$, which was not enough for a 1 G-bit DRAM device. Therefore, the choice of electrode materials may become as important as the choice of insulators for DRAM development. Besides, the materials such as platinum, ruthenium, ruthenium oxide, and iridium oxide have the disadvantages of high costs,

difficulties in dry etching process, and generation of highly toxic gases which were formed during the reactive ion etching (RIE) processing of these materials. The new bottom electrode was introduced, which used a metallic buffer on a capacitor stack built on TiN/Si substrate (Au/BST/M/TiN/Si). This capacitor stack was integrated to silicon for DRAMs.

The ferroelectric materials such as strontium titanate (STO) and barium titanate (BTO) were used in microwave devices. STO/YBCO (YBCO is a high temperature superconductor) structures found their applications in coplanar waveguide devices. YBCO/STO/LAO (conductor/ferroelectric/dielectric) thin film multiple-layer structures could be applied to Ku- and K-band satellite communication. They were used as microwave phase shifters, too. BST was used in tunable microwave devices such as voltage tunable phase shifter, oscillators, filters, and parametric amplifiers. One of the problems of using BST for microwave devices was a high loss tangent. BST with various dopants were investigated to optimize the properties of BST in very high frequencies.

A new way to model Metal-Ferroelectric-Semiconductor Field Effect Transistor was introduced by Todd MacLeod and Fat Duen Ho. This is different from the models proposed previously.

It was concluded that both PZT and SBT are the major ferroelectric materials used in developing FeRAM. For SBT the problems of high processing temperature and barrier material for bottom electrodes had been solved. For PZT the combat against fatigue and imprint by using Ir based top electrode had been successful. Besides, PZT films doped with La, Nb and Sb showed the improvement of its fatigue properties. The progress of BST capacitors in the giga-bit scale dynamic random-access memories and on-chip capacitors for RF devices was made. The choice of electrode materials is the critical issue for BST capacitors. The application of

ferroelectric materials such as STO and BTO to microwave devices makes the study of integrated ferroelectrics even more important.

It is recommended that the research and development of Metal-Ferroelectric-Semiconductor Field Effect Transistors and their application in nonvolatile memories should be further pursued.

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Appendix I

Modeling Metal-Ferroelectric-Semiconductor Field Effect Transistor

Integrated Ferroelectrics, 1998, Vol. 21, pp. 127–143
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MODELING OF METAL-FERROELECTRIC-SEMICONDUCTOR FIELD EFFECT TRANSISTORS

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The characteristics for a MFSFET (metal-ferroelectric-semiconductor field effect transistor) is very different than a conventional MOSFET and must be modeled differently. The drain current has a hysteresis shape with respect to the gate voltage. The position along the hysteresis curve is dependent on the last positive or negative polling of the ferroelectric material. The drain current also has a logarithmic decay after the last polling. A model has been developed to describe the MFSFET drain current for both gate voltage on and gate voltage off conditions. This model takes into account the hysteresis nature of the MFSFET and the time dependent decay. The model is based on the shape of the Fermi-Dirac function which has been modified to describe the MFSFET's drain current. This is different from the model proposed by Chen et. al.[1] and that by Wu[2].

Keywords: ferroelectric transistors; hysteresis modeling; ferroelectric time decay

INTRODUCTION

Several Integrated Circuits containing PZT channel metal-ferroelectric-semiconductor field effect transistors (MFSFET) were obtained from Radiant Technologies Incorporated located in Albuquerque, New Mexico. The transistors were fabricated from silicon but have the channel fabricated from thin film PZT. This allows the gate to source voltage to either open or close the channel. The channel will remain opened or closed even after the gate to source voltage is removed. These transistors were characterized by recreating a circuit and reproducing the data as described in a correspondence from Radiant Technologies in April, 1993[5][6].

TESTING THE MFSFET

Test Setup

The tests were performed by setting up the circuit shown in Figure 1.

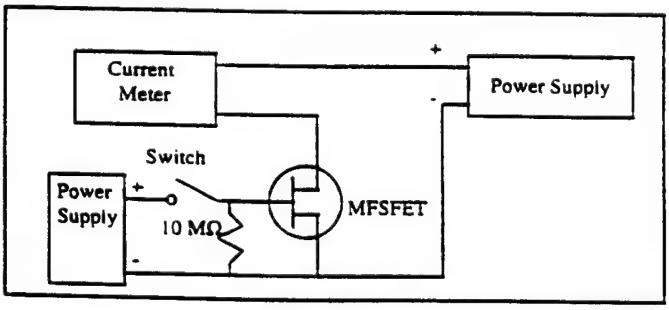

FIGURE 1. Ferroelectric Field Effect Transistor Test Setup

With the Drain to Source voltage held constant, a series of pulses were sent to the Gate of the MFSFET. To establish the initial conditions, a -8.0 volt polling pulse was applied. This polling pulse saturated the ferroelectric channel in the open position. The Gate pulses started at 0.0 volts and was increased by 0.50 volts until the pulses reached +8.0 volts. The amplitude of the pulses was then decreased by 0.50 volts until 0.0 volts was again reached. Then a +8.0 polling pulse was applied. This polling pulse place the ferroelectric channel into saturation with the channel closed. Negative pulses were then applied every 0.50 volts from 0.0 volts to -8.0 volts and back to 0.0 volts. Figure 2 shows the series of pulses that were applied to the MFSFET Gate.

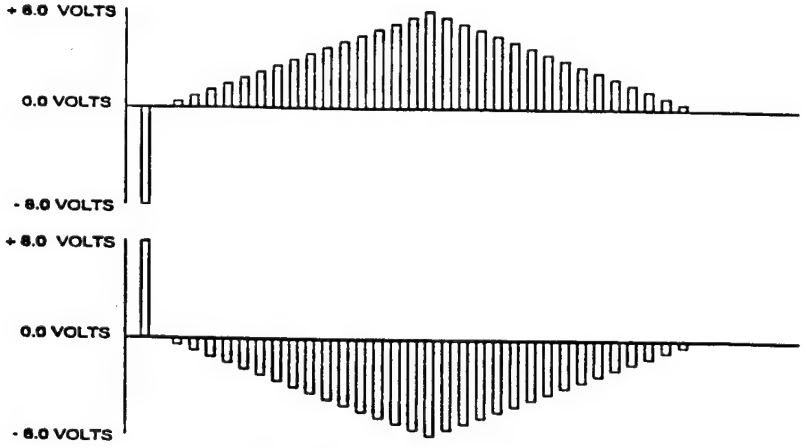

FIGURE 2 Pulse Pattern Sent to MFSFET Gate

When the switch is thrown applying voltage to the Gate, a reading is made of the channel current. This is described as the "On" current because it is the current flowing when the MFSFET is actively be operated. The switch is then closed, removing any voltage to the Gate (the 10 megaohm resistor insures that the Gate and Source are at the same voltage when the switch is open). A second reading of channel current is then made. This current is described as the "Off" current because the transistor is not actively being operated. This "Off" current will continue to flow as long as a voltage is applied from the Drain to the Source.

The Drain to Source voltage is nominally set at 0.4 volts. To characterize the effects of Drain to Source voltage on channel polarization retention, the voltage was varied from 0.1 volts to 0.5 volts. After the Drain to Source voltage was set, the gate was pulsed with pulses in the same manner as was done to characterize the effects of Gate voltage. Figure 3 shows the effects of varying the Drain to Source voltage on the MFSFET transistor.

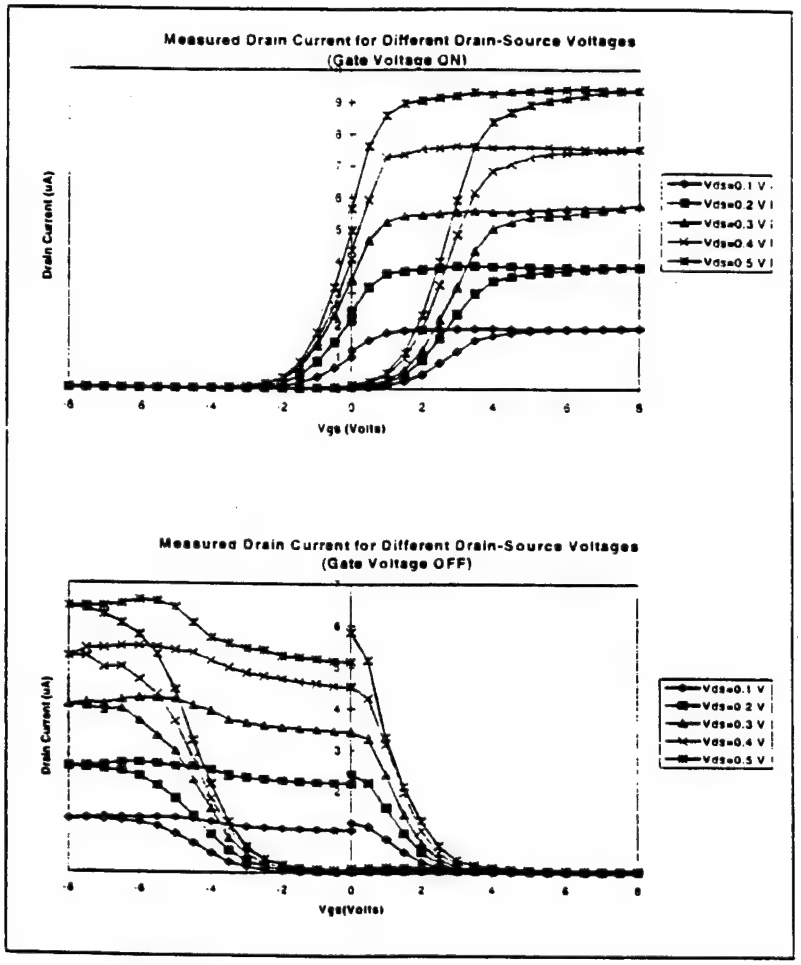

Figure 3 Ferroelectric MFSFET Characterization Data Resulting from Variation in Drain to Source Voltage

Remnant Current Retention

The ferroelectric transistor must be able to store data for long periods of time. To measure the polarization retention characteristics of the MFSFET, measurements were made of the channel current over long periods of time. The channel was set to the open state by sending a -8.0 volt pulse to the Gate. This causes the ferroelectric channel to be saturated. The voltage to the Gate is removed and the current is measured for up to 7000 seconds. Figure 4 shows the retention data for the ferroelectric MFSFET.

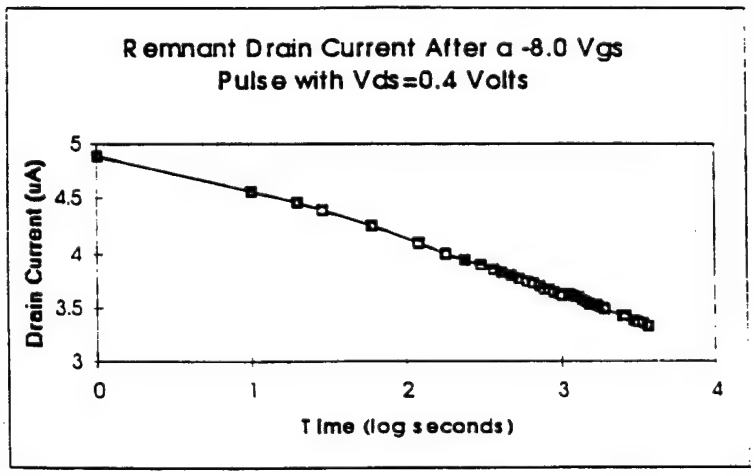

Figure 4 Ferroelectric MFSFET Remnant Current Data

MODELING OF MFSFET's

The MFSFET retention data shows that the degradation of the Drain current is linear with the logarithm of time. The relationship can be given by the equation:

$$I_D = A - B \log (\text{time}) \qquad (1)$$

Where:

I_D = the current flowing through the Drain

A = the initial current flow through the Drain

B = the coefficient that gives the rate of current decay

Using the least squares method of data reduction the coefficients A and B can be calculated. Table 1 shows the calculation of A and B for the transistor at room temperature with Vds at 0.4 volts .

N	Time (s)	I_D (mA)	Log (t)	Log $(t)^2$	Log (t)* I_D
1	1	4.89	0	0	0
2	10	4.56	1	1	4.56
3	100	4.06	2	4	8.12
4	500	3.79	2.69897	7.28444	10.2290963
5	1000	3.6	3	9	10.8
6	2000	3.47	3.30103	10.8968	11.4545741
7	4000	3.32	3.60206	12.9748	11.9588392
N=7	Sum:	27.69	15.6021	45.1561	57.1225096
			$I_{D\ ave}$ =	3.95571	

A	B	$I_{D\ est}$	r_{ss}	t_{ss}	$R^2=(t_{ss}-r_{ss})/t_{ss}$
4.942	**-0.44261**	4.942226	0.00273	0.87289	**0.99545334**
		4.499619	0.00365	0.36516	
		4.057012	8.9E-06	0.01088	
		3.747643	0.00179	0.02746	
		3.614405	0.00021	0.12653	
		3.481167	0.00012	0.23592	
		3.347929	0.00078	0.40413	
		Sum:	**27.69**	**0.0093**	**2.04297143**

Table 1 Calculation of retention Coefficients for Ferroelectric Field Effect Transistors

MODELING OF THE MFSFET

There are two types of standard Field Effect transistors; Enhancement mode and Depletion mode. An Enhancement mode MFSFET allows no current to flow between the source and the drain when the gate voltage is zero. As the gate voltage increases from zero, the source drain current increases until it is saturated. A Depletion mode MOSFET allows current to flow between the source and drain when the gate voltage is zero. As the gate voltage increases from zero, the source-drain current is pinched off until it reaches zero. The ferroelectric MFSFET acts as both an enhancement mode and a depletion mode transistor. If the gate has received a negative pulse, negative polled, then the MFSFET will act as depletion mode transistor. If the MFSFET has received a positive pulse, positive polled, it will behave as an enhancement mode MOSFET.

Two separate models must be used to characterize an MFSFET, one enhancement mode model and a depletion mode model.

The first attempt to model the MFSFET was to use the standard MOSFET model. For a depletion mode MOSFET, Boylestad[3] gives the equation for the drain current

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (2)$$

Where

I_D = drain current

I_{DSS} = the drain-source current with the gate and source shorted

V_{GS} = the gate source voltage

V_p = the pinch-off voltage where I_D equals 0

This equation yields a the following curve depicting drain current versus gate voltage .

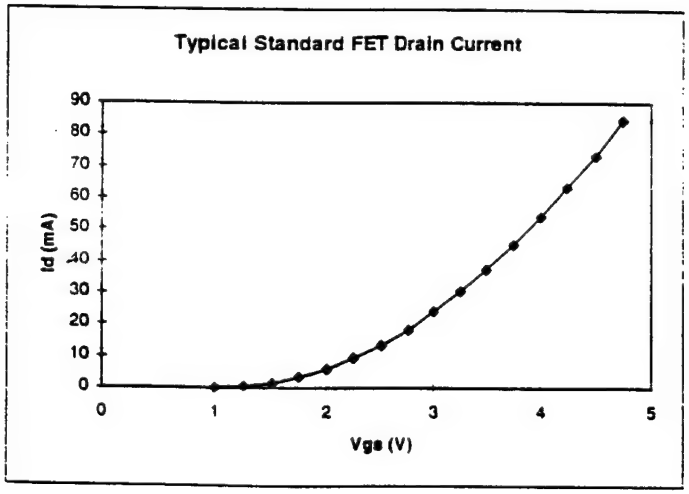

FIGURE 5 Drain current from Standard MOSFET Model

This curve does not fit the MFSFET drain current curve at all. Even though the MFSFET is structurally very similar to a standard MOSFET, the current characteristics are very different. A different type of equation is needed to model the MFSFET. The equation that has the most similar shape to the MFSFET is the Fermi-Dirac function. This function describes the distribution of electrons at different energy levels. Lo[4] gives the Fermi-Dirac function as

$$f(E) = \frac{1}{e^{(E-E_f)T} + 1} \tag{3}$$

Where

f(E) = the probability of finding an electron at Energy E at Temperature T

E_f = called the Fermi level for a particular electron shell

T = the absolute temperature in Kelvin

The use of this equation to describe the drain current in an MFSFET is only because of its shape and not because drain current is related to the distribution of electrons within an atom's energy shells. The Fermi-Dirac function must be changed to be used to model the MFSFET. The following equation was created to model the MFSFET drain current with the gate voltage ON.

$$I_D = \frac{I_{DSAT}}{e^{k(V_P - V_{GS})} + 1} \tag{4}$$

and

$$I_D = \frac{I_{DSAT} - B * Log(t_1)}{e^{k(V_{GS} - V_P)} + 1} \tag{5}$$

when the gate voltage is OFF.

Where

I_D = the drain current

I_{DSAT} = the value for the drain current when the MFSFET is saturated

B = the decay coefficient

t_1 = the time in seconds since the last polling

Vgs = the gate to source voltage

Vp = the gate voltage at which half of the saturation current is achieved (Each MFSFET has two Vp's one for the negatively polled current and one for the positively polled current thus giving the hysteresis characteristic.)

k = a constant that defines the rate of change of the function

For the MFSFET in this research, the following values for the variables are used to model the drain current.

For the gate voltage ON

Vp = 2.5 V for positively polled

Vp = -0.5 V for negatively polled

k = 1.7

I_{DSAT} = 9.0 uA for Vds= 0.5 V

7.2 uA for Vds= 0.4 V

5.3 uA for Vds= 0.3 V

3.5 uA for Vds= 0.2 V

1.8 uA for Vds= 0.1 V

For the model with the gate voltage OFF

Vp = -4.2 V for positively polled

Vp = 1.5 V for negatively polled

k=1.7

I_{DSAT} = 6.5 uA for Vds= 0.5 V

5.2 uA for Vds= 0.4 V

4.0 uA for Vds= 0.3 V

2.5 uA for Vds= 0.2 V

1.2 uA for Vds= 0.1 V

t_1= 1 second if immediately after polling

or

t_1 is increased by 20 seconds for each measurement

Using the above values for the drain current model yields the following curves shown in figures 6 and 7.

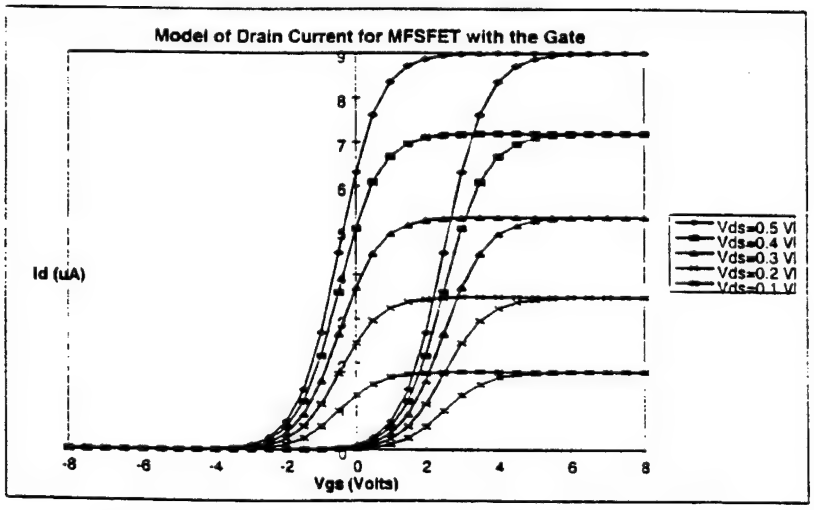

FIGURE 6 Predicted Drain Current using MFSFET Model (Gate ON)

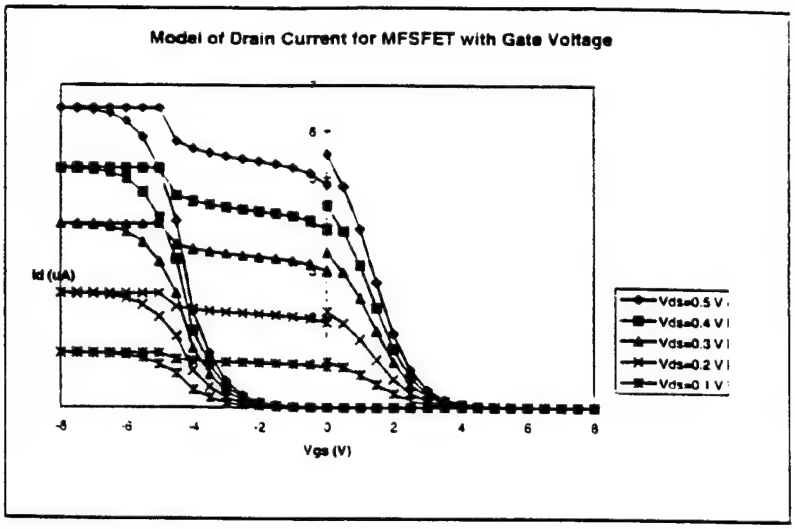

FIGURE 7 Predicted Drain Current using MFSFET Model (Gate OFF)

When these curves are compared with the observed data in Figure 3, the predicted drain current is very close the measured data. The Data used to create the MFSFET model is shown in Table 2.

Vgs	Id=.5	Id=.4	Id=.3	Id=.2	Id=.1	k	Vo	Id_{sat} .5	0.4	0.3	0.2	0.1	Delay time
0	5.495	4.396	3.382	2.113	1.015	1.7	1.5	5.924	4.739	3.646	2.278	1.094	11
1	3.892	3.113	2.396	1.497	0.719	1.7	1.5	5.556	4.444	3.419	2.136	1.026	51
2	1.622	1.297	0.998	0.624	0.299	1.7	1.5	5.417	4.333	3.334	2.083	1	91
3	0.386	0.309	0.238	0.148	0.071	1.7	1.5	5.329	4.263	3.28	2.049	0.984	131
4	0.074	0.059	0.046	0.028	0.014	1.7	1.5	5.265	4.212	3.241	2.024	0.972	171
5	0.017	0.014	0.01	0.006	0.003	1.7	1.5	6.5	5.2	4	2.5	1.2	1
6	0.003	0.002	0.002	0.001	6E-04	1.7	1.5	6.5	5.2	4	2.5	1.2	1
7	6E-04	5E-04	3E-04	2E-04	1E-04	1.7	1.5	6.5	5.2	4	2.5	1.2	1
8	1E-04	8E-05	6E-05	4E-05	2E-05	1.7	1.5	6.5	5.2	4	2.5	1.2	1
7	3E-08	3E-08	2E-08	1E-08	6E-09	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
6	2E-07	2E-07	1E-07	7E-08	4E-08	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
5	1E-06	8E-07	6E-07	4E-07	2E-07	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
4	5E-06	4E-06	3E-06	2E-06	9E-07	1.7	-4.2	5.769	4.615	3.55	2.218	1.065	21
3	3E-05	2E-05	2E-05	1E-05	5E-06	1.7	-4.2	5.513	4.41	3.393	2.12	1.018	61
2	1E-04	1E-04	9E-05	5E-05	3E-05	1.7	-4.2	5.392	4.313	3.319	2.073	0.996	101
1	8E-04	6E-04	5E-04	3E-04	1E-04	1.7	-4.2	5.311	4.249	3.269	2.042	0.981	141
0	0.004	0.003	0.003	0.002	8E-04	1.7	-4.2	5.252	4.201	3.232	2.019	0.97	181
-1	0.022	0.018	0.014	0.009	0.004	1.7	-4.2	5.204	4.162	3.203	2.001	0.961	221
-2	0.12	0.096	0.074	0.046	0.022	1.7	-4.2	5.164	4.13	3.178	1.985	0.954	261
-3	0.59	0.472	0.363	0.227	0.109	1.7	-4.2	5.129	4.103	3.157	1.972	0.947	301
-4	2.12	1.696	1.305	0.815	0.392	1.7	-4.2	5.099	4.079	3.139	1.961	0.942	341
-5	5.172	4.138	3.183	1.989	0.955	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
-6	6.209	4.967	3.821	2.388	1.146	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
-7	6.445	5.156	3.966	2.479	1.19	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
-8	6.49	5.192	3.994	2.496	1.198	1.7	-4.2	6.5	5.2	4	2.5	1.2	1
-7	6.5	5.2	4	2.5	1.2	1.7	1.5	6.5	5.2	4	2.5	1.2	1
-6	6.5	5.2	4	2.5	1.2	1.7	1.5	6.5	5.2	4	2.5	1.2	1
-5	6.5	5.2	4	2.5	1.2	1.7	1.5	6.5	5.2	4	2.5	1.2	1
-4	5.608	4.486	3.451	2.156	1.035	1.7	1.5	5.608	4.486	3.452	2.156	1.035	41
-3	5.442	4.353	3.35	2.092	1.005	1.7	1.5	5.445	4.355	3.351	2.093	1.005	81
-2	5.334	4.267	3.283	2.051	0.985	1.7	1.5	5.348	4.278	3.292	2.056	0.988	121
-1	5.205	4.164	3.204	2.001	0.961	1.7	1.5	5.28	4.223	3.25	2.03	0.975	161
0	4.848	3.878	2.984	1.864	0.895	1.7	1.5	5.226	4.181	3.217	2.009	0.965	201

TABLE 2 Data used to create MFSFET model (Gate Off)

CONCLUSIONS

Because of the hysteresis characteristic of the MFSFET the model is complex, but by using the modified Fermi-Dirac shaped function a very accurate model of the MFSFET is possible.

Acknowledgments

One of the authors, Fat Duen Ho, would like to acknowledge his appreciation to the U.S. Army Space and Missile Defense Command and Physitron Inc., especially Mr. Alfred C. Kuehl, for the support they gave us on the testing of Metal-Ferroelectric-Semiconductor FET's. He would also express his thanks to Mr. Robert Suizu and Mr. Joe Evans of Radiant Technologies Inc. for providing the MFSFET's and for their helpful discussions concerning the testing procedures. Thanks also due to Mr. Morris Kea, an undergraduate student at UAH in 1995, for his assistance in testing the MFSFET's.

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Appendix II

Integrating Partial Polarization Into a Metal-Ferroelectric-Semiconductor Field Effect Transistor Model

INTEGRATING PARTIAL POLARIZATION INTO A METAL-FERROELECRIC-SEMICONDUCTOR FIELD EFFECT TRANSISTOR MODEL

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The ferroelectric channel in a Metal-Ferroelectric-Semiconductor Field Effect Transistor (MFSFET) can partially change its polarization when the gate voltage nears the polarization threshold voltage as shown by Aizawa[1]. This causes the MFSFET Drain current to change with repeated pulses of the same gate voltage near the polarization threshold voltage. A previously developed model [2] assumed that for a given gate voltage and channel polarization, a single Drain current value would be generated. The earlier model accurately predicts the Drain current given a series of increasing and decreasing pulses, but does not predict the current well for a series of random pulses. A study has been done to characterize the effects of partial polarization on the Drain current of a MFSFET. These effects have been incorporated into a more comprehensive mathematical model of the MFSFET. The model takes into account the hysteresis nature of the MFSFET and the time dependent decay as well as the effects of partial polarization.

Keywords: ferroelectric transistors, partial polarization

INTRODUCTION

A previous model[2] was developed to characterize the drain current for a metal-ferroelectric-semiconductor field effect transistor (MFSFET). This model accurately predicted the drain current given a series of increasing and decreasing gate pulses. It did not, however, accurately describe the drain current given a random series of pulses. A new model was developed that would take into account the effect of partial polarization.

PREVIOUS MODEL

The previous model calculated the Drain Current for a MFSFET to a high level of accuracy for both conditions of gate voltage On and Off and for the current decay over time. However, this model con not accurately predict the MFSFET Drain current given a random series of Gate pulses with the Gate voltage Off. This model can still accurately predict the Drain current with the Gate voltage On.
MFSFET Drain current Model with the Gate voltage On :

$$I_D = \frac{I_{DSAT}}{e^{k(V_p - V_{gs})} + 1} \qquad (1)$$

where

I_{DSAT} = the saturation current for the MFSFET
k = rate of change constant
V_p = Voltage threshold for polarization change
V_{gs} = Gate to Source voltage

The model gate voltage is On is much more straight forward than gate voltage Off because while the Gate voltage is on there is no logarithmic decay and there is no partial polarization effect. The model was verified by comparing it to measured data from a MFSFET obtained from Radiant Technologies. The figure below shows the output generated by the model.

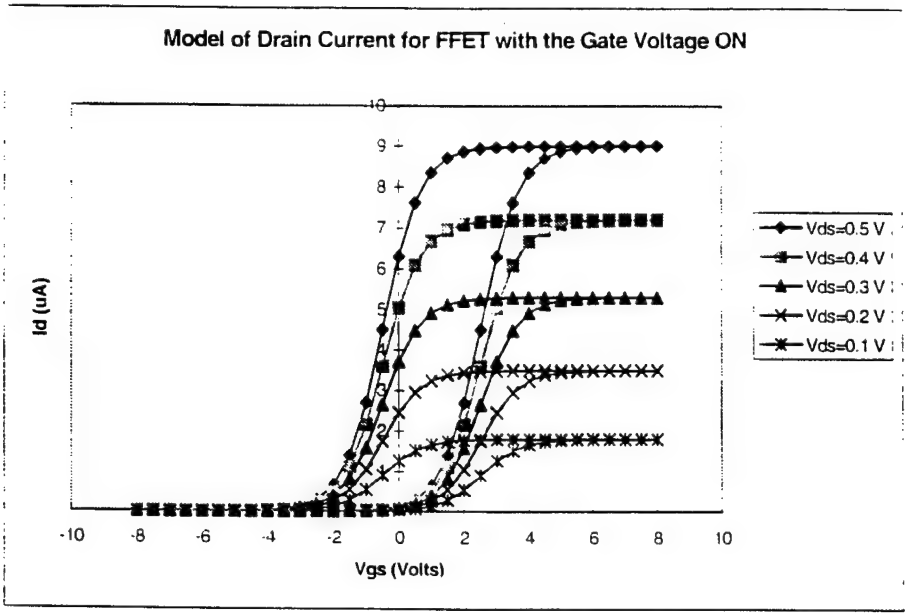

FIGURE 1 MFSFET Drain Current with Gate Voltage ON

The previous model for the gate voltage OFF was:

$$I_D = \frac{I_{DSAT} - B * Log(t_1)}{e^{k(V_{gs}-V_p)} + 1} \qquad (2)$$

Where

I_D = the drain current

I_{DSAT} = the value for the drain current when the MFSFET is saturated

B = the decay coefficient

t_1 = the time in seconds since the last polling

Vgs = the gate to source voltage

Vp = the gate voltage at which half of the saturation current is achieved (Each MFSFET has two Vp's one for the negatively polled current and one for the positively polled current thus giving the hysteresis characteristic.)

k = a constant that defines the rate of change of the function

This model assumes a known amount of polarization exists in the ferroelectric material before each pulse. This is true only for a standardized set of pulses. In general, pulses could be of random magnitude and direction. Therefore, this model can not accurately predict the drain current.

PARTIAL POLARIZATION

The reason that the previous model does not accurately predict the Drain current is that it does not accurately model the effects of partial polarization. Partial polarization is caused by a pulse, which is less than the threshold voltage, but still changes the ferroelectric polarization to some degree. Also, the amount of polarization that is changed varies for a given gate voltage with the amount of polarization already existing in the ferroelectric. This effect was shown by Aizawa et. al [1]. The drain current, which is proportional to the ferroelectric polarization, was measured for repeated pulses of the same gate voltage. The figure below shows the Drain current versus the natural log of the number of pulses.

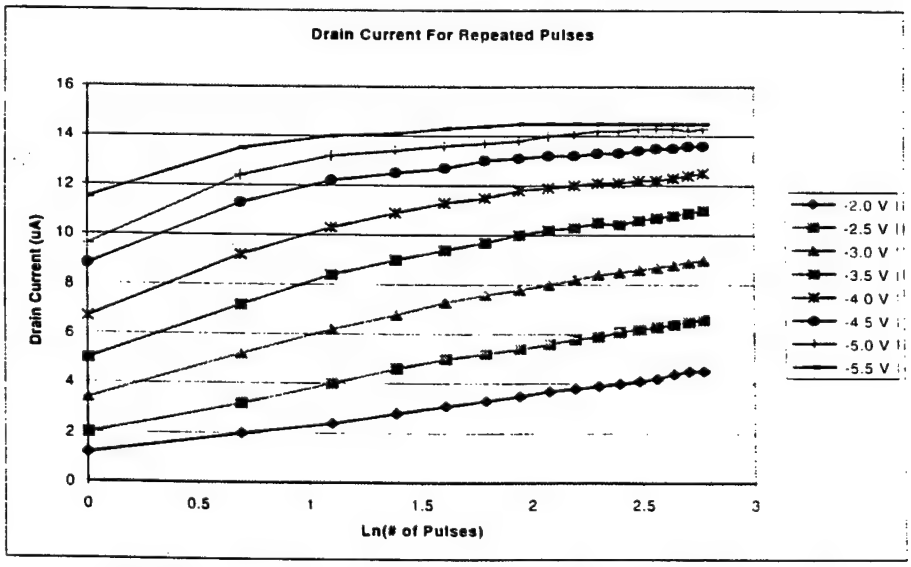

FIGURE 2 The Effect of Repeated Pulses on Drain Current

The figure shows that the polarization increases logarithmically for repeated pulses of the same voltage. A similar phenomenon occurs for decreasing drain current with positive pulses. The slope decreases when the current becomes large because the effect of decay between pulses becomes greater.

INTEGRATED MODEL

A model has been created that can accurately predict the Drain current given a random series of Gate pulses both in voltage and time. The model has the form:

$$I_D = k_1 + k_2 * \ln(e^{\frac{I_D^* - k_1}{k_2}} + 1) \quad (3)$$

Where:

$$k_1 = -3.24 * V_{gs} - 6.15 \quad (4)$$

For negative pulses and

$$k_1 = -5.14 * V_{gs} + 15.93 \quad (5)$$

For positive pulses

$$k_2 = -0.65 * V_{gs} \quad (6)$$

For negative pulses and

$$k_2 = 0.025 * V_{gs}^2 - 0.425 \quad (7)$$

For positive pulses

I_D^* is the calculated Drain current just prior to the Gate pulse being made including current decay with time.

Model Verification

This model has been used to accurately predict the Drain Current given a series of random Gate pulses in voltage polarity and time between pulses. The figure below shows the series of gate pulses that was sent to the MFSFET from Radiant Technologies. The Drain to Source voltage was kept at a constant 0.4 VDC.

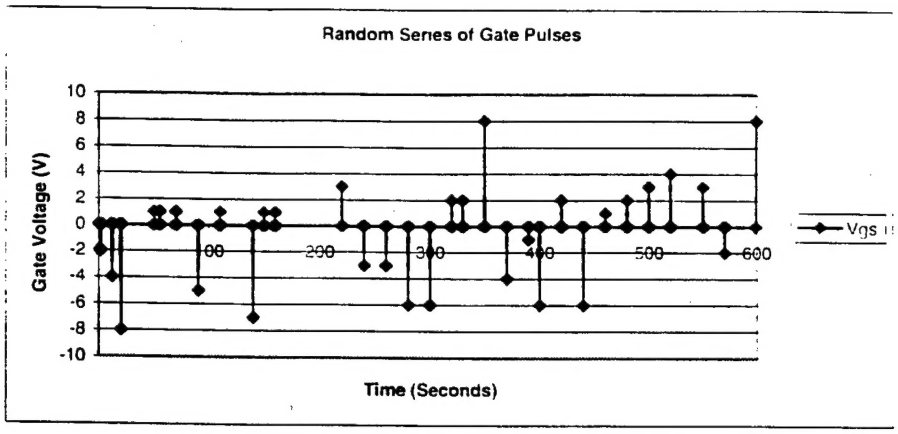

FIGURE 3 Random Series of Gate Pulses

The model generated this plot of the Drain current after the Gate voltage is off:

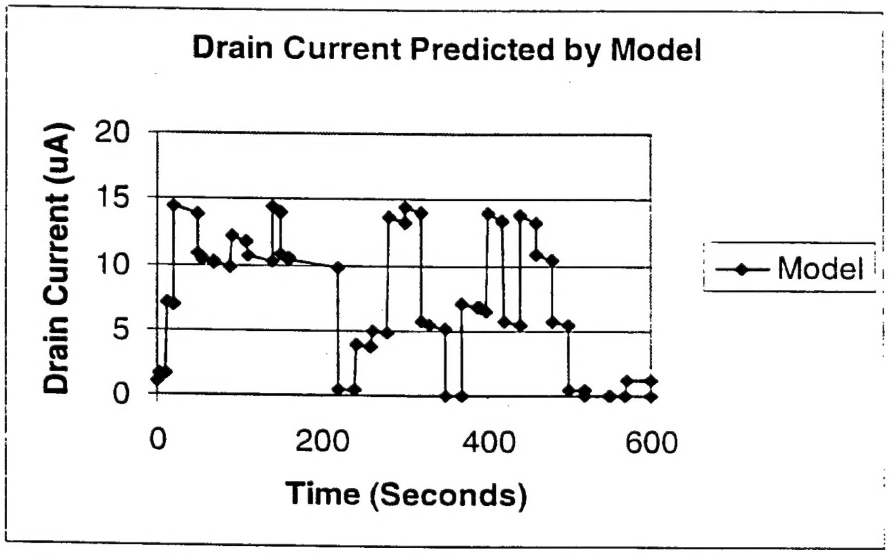

FIGURE 4 Model Prediction of Drain Current

Below is a table showing the individual components of the model as well as the measured Drain current. The graphs show the Drain current

Time	ID	Measured Current	Vds	K1	K2	K3	K4	Idsat
1	1.076534	[illegible]	-2	0.33	1.3	26.21	-0.325	14.5
2	1.657226	1.5	-2	0.33	1.3	26.21	-0.325	
12	7.139613	6.8	-4	6.81	2.6	36.49	-0.025	
20	14.5	14.2	-8	19.77	5.2	57.05	1.175	
50	10.78639	10.5	1	-9.39	-0.65	10.79	-0.4	
55	10.43439	10.2	1	-9.39	-0.65	10.79	-0.4	
70	10.22803	9.9	1	-9.39	-0.65	10.79	-0.4	
90	12.19065	12.3	-5	10.05	3.25	41.63	0.2	
110	10.70262	10.2	1	-9.39	-0.65	10.79	-0.4	
140	14.5	14.3	-7	16.53	4.55	51.91	0.8	
150	10.78738	10.2	1	-9.39	-0.65	10.79	-0.4	
160	10.39772	9.8	1	-9.39	-0.65	10.79	-0.4	
220	0.50833	1.2	3	-15.87	-1.95	0.51	-0.2	
240	3.935066	3.9	-3	3.57	1.95	31.35	-0.2	
260	5.028827	5.1	-3	3.57	1.95	31.35	-0.2	
280	13.71187	13.2	-6	13.29	3.9	46.77	0.475	
300	14.5	13.9	-6	13.29	3.9	46.77	0.475	
320	5.649441	5.2	2	-12.63	-1.3	5.65	-0.325	
330	5.402383	4.9	2	-12.63	-1.3	5.65	-0.325	
350	0	0	8	-32.07	-5.2	-25.19	1.175	
370	6.99285	6.2	-4	6.81	2.6	36.49	-0.025	
390	6.715145	5.9	-1	-2.91	0.65	21.07	-0.4	
400	13.92159	12.9	-6	13.29	3.9	46.77	0.475	
420	5.649144	4.9	2	-12.63	-1.3	5.65	-0.325	
440	13.7773	13.2	-6	13.29	3.9	46.77	0.475	
460	10.78074	9.5	1	-9.39	-0.65	10.79	-0.4	
480	5.641388	4.8	2	-12.63	-1.3	5.65	-0.325	
500	0.494472	0.7	3	-15.87	-1.95	0.51	-0.2	
520	0	0.1	4	-19.11	-2.6	-4.63	-0.025	
550	0.343512	0	3	-15.87	-1.95	0.51	-0.2	
570	1.231026	1.2	-2	0.33	1.3	26.21	-0.325	
600	0	0	8	-32.07	-5.2	-25.19	1.175	

TABLE 1 Predicted and Actual MFSFET Data

The model accurately predicts the current measured when the random set of pulses were sent to the gate of a MFSFET provided by Radiant Technologies.

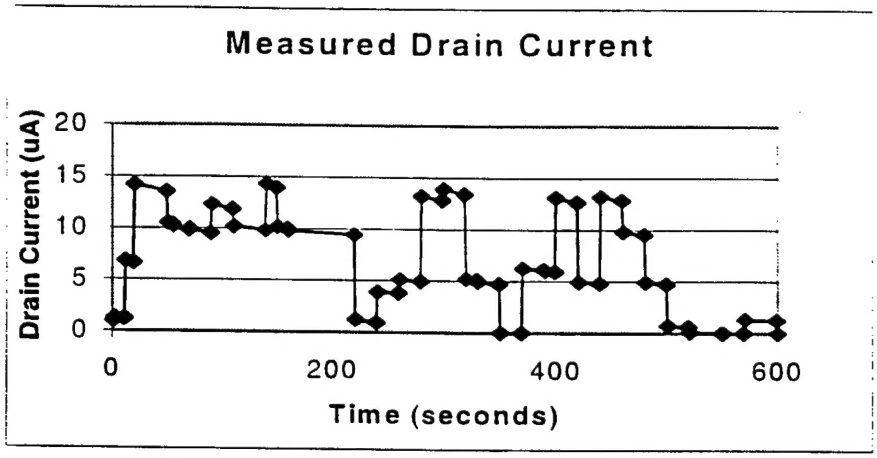

FIGURE 5 Measured Drain Current

CONCLUSIONS

The improved model of the MFSFET accurately characterizes the drain current given any series of Gate pulses. This model uses a different approach to modeling the MFSFET than that proposed by Chen et. Al.[3] and that by Wu[4]. It takes in to account the hysteresis nature of the MFSFET as well as the logarithmic decay and partial polarization of the ferroelectric channel.

Acknowledgments

We would like to acknowledge Mr. Robert Suizu and Mr. Joe Evans of Radiant Technologies Inc. for providing the MFSFET's and for their helpful discussions concerning the testing procedures. We would like to acknowledge our appreciation to the U.S. Army Space and Missile Defense Command, especially Mr. Alfred C. Kuehl, for the support they gave us on the testing of Metal-Ferroelectric-Semiconductor FET's.

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